WIDEBAND GaAs FOUR QUADRANT MULTIPLIER

C. Ryan*, D. Hartman*, J.M. Frary† and C.E. Weitzel†

Motorola, Inc.

*CRF, 75 W. Olive
Gilbert, AZ 85234

†SRDL, 5005 E. McDowell
Phoenix, AZ 85008

Abstract

A four quadrant multiplier has a variety of high frequency, signal processing applications (phase detection, modulation, and frequency conversion). This paper describes work undertaken to design, model, fabricate, and test a GaAs monolithic four quadrant multiplier which utilizes dual-gate FETs.

The multiplier was fabricated using n-type expitaxial GaAs on a high resistivity substrate.

Introduction

One of the fundamental building blocks in any wideband communications system is the multiplier, since it offers a means by which two analog signals may be combined, or mixed to give a resultant product vector.

Examples of the applications for this device include phase detectors, modulators, and frequency conversion. This paper describes the development of a GaAs monolithic four quadrant multiplier suitable for use up to X band frequencies. It can therefore be used to replace the more conventional discrete diode type of mixers. the design presented here is similar to that presented in [1] as well as the bipolar multiplier in current use at lower frequencies [2]. The multiplying action is achieved by controlling the channel impedance of the lower set of MESFET's illustrated in Figure 2.1. This method of obtaining gain control is different than the bipolar and the GaAs FET transconductance multiplier[3]. The variable channel impedance mode provides for better linearity than the variable transconductance mode as well as permitting all inputs to be biased at a DC ground potential.

The design presented in this report is configured for operaton in either the single ended or the differential mode. The differential mode of operation provides a 20 dB balance, whereas, the single ended mode of operation has a balance of 10 dB.

Measured as well as simulated results indicate a useful frequency response up to 8 GHz and an on-to-off ratio of 20 dB for a 50 ps rise time input signal. Primary focus of the effort to date has been on the circuit modeling and characterization of its fundamental performance parameters such as DC response, square law operation, forward and reverse transfer ratios and transient responses.

Theoretical Circuit Response

Circuit modeling for the four-quadrant multiplier was performed using the SPICE JFET model. This was done largely because of the availability of the model and the usefulness of SPICE in obtaining D.C. and A.C. data, as well as transient data. While the limitations of the SPICE JFET model in modeling GaAs MESFET's is recognized [4], it is believed that the error incurred in using this model for the circuits thus far implemented is of the same order of magnitude as or less than the processing uncertainties.

The four quadrant multiplier circuit (Figure 2.1) can be most easily understood by considering each dual gate FET as two single gate FET's connected in cascode. There the bias conditions of the circuit are chosen so that the upper tier transistors are biased in the saturated region and the lower tier is biased so they act as voltage variable resistors. Transistor MC is a current source which draws about 12.5 mA. The impedance of this current source as a function of frequency is a useful measure of the circuits overall balance for single ended input signals.

CH1875-4/83/0000-0005 $1.00 © 1983 IEEE

Quick reference to Figure 2.1 shows that the four quadrant multiplier can be thought of as two differential amplifiers with crossed drains. The transconductance, g_{md}, of each differential amplifier can be written as a function of the voltage variable resistance, R, of the lower tier transistors. Setting G = 1/R, the result can be expressed as:

$$g_{md} = \frac{-\frac{G}{V_p}\sqrt{I_{d1}I_{dss}}}{G - \frac{2}{V_p}\sqrt{I_{d1}I_{dss}}} \qquad (2.1)$$

This shows that if G is controlled by the input to the lower tier of transistors, then the output voltage is, to a good approximation, the scaled product of the inputs.

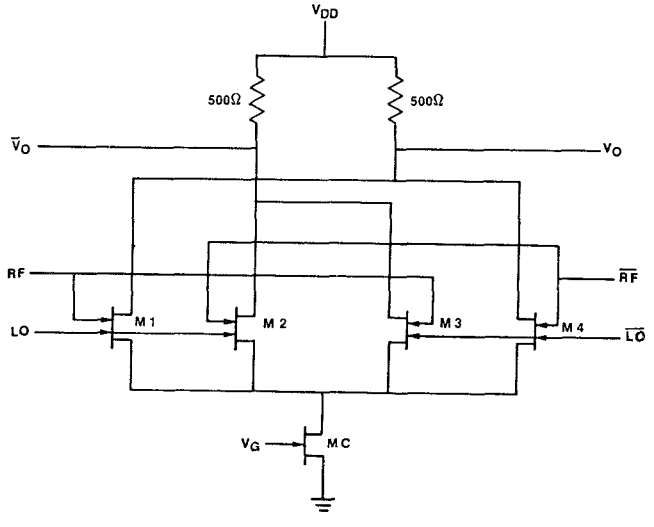

Figure 2.1 Four Quadrant Multiplier Circuit Schematic

The result in equation 2.1 applies strictly to the small signal domain and is included here to illustrate the basic concept of the MESFET four quadrant multiplier. To understand more completely the expected performance of the circuit, simulations were performed using the SPICE circuit simulation package. As previously noted the MESFET transistors were simulated using the SPICE JFET model. D.C. transfer curves were computed on the circuit to obtain its gain linearity and expected square-law and anti-square law response: Figure 2.2 shows a plot of the computed differential gain of the multiplier circuit as a function of differential input voltage, also, differential signals of equal magnitude and with both equal and opposite sign were applied to the RF and LO ports. The data from these tests is plotted in Figures 2.2. The portion of the square-law characteristic that lies in the first quadrant is plotted in Figure 2.4 on log-log scales. Also plotted is a best fit line with the slope of a perfect sqaure-law device. The error between the multiplier circuit data and the best fit line is plotted in Figure 2.5. Here a high degree of expected multiplier linearity is exhibited.

Finally, measurements of RF response are shown in Figures 2.6 through 2.8. Figure 2.6 shows the computed current source (MC) impedance vs. frequency. The impedance value has been calculated for the case where the transistor MC has its source grounded (R_E=Ø) and where a 1ØØ_ resitance has been inserted between the source of MC and ground. This illustrates the effect of a source resistance and indicates a way in which one can increase the current source impedance, thereby benifically affecting multiplier balance. Figure 2.7 shows a plot of computed upper gate input impedance (S_{11}) vs. frequency for various lower gate voltage. Finally, Figures 2.8a and 2.8b show plots of computed reverse gain (S_{21}), which is feedthrough from the multiplier output to the upper gate, vs. frequency.

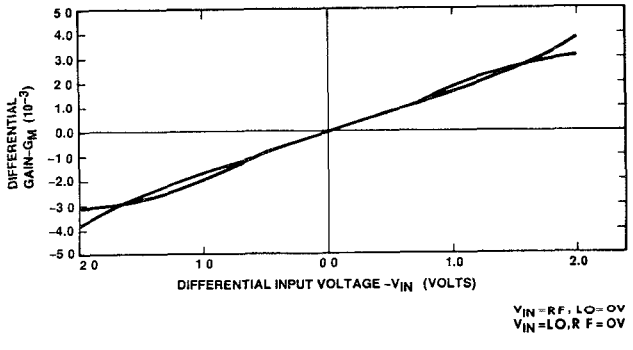

Figure 2.2 Multiplier Differential Transconductance as a function of input differential voltage for RF and for LO ports

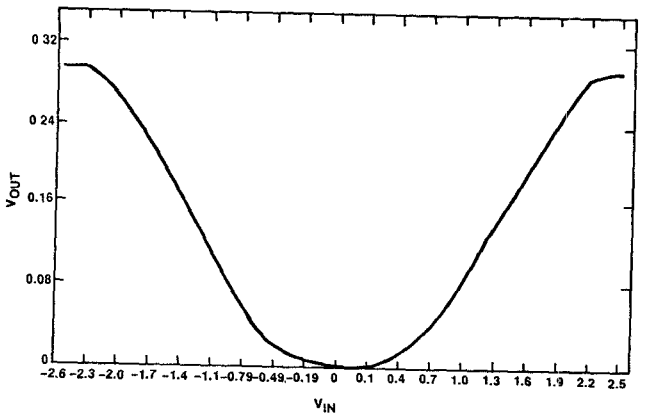

Figure 2.3 Computed differential square law response of the multiplier circuit

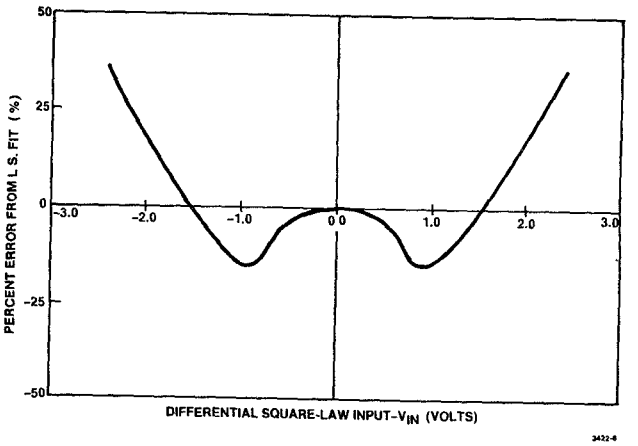

Figure 2.5 Computed square law error term, obtained from data of Figure 2.3

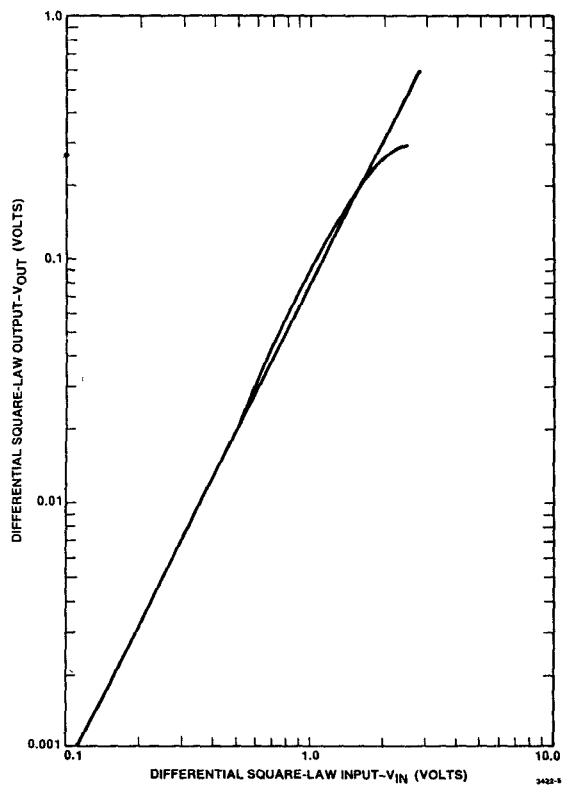

Figure 2.4 Square law response of positive half of Figure 2.4, plotted on log-log paper, against a perfect sqaure law response

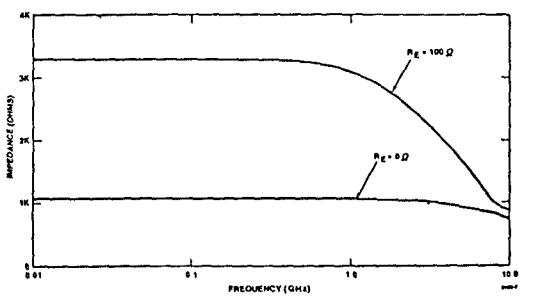

Figure 2.6 Computed impedance of the current source MC vs. frequency for a grounded source (R_S=Ø) and for a source resistnace of 1ØØΩ

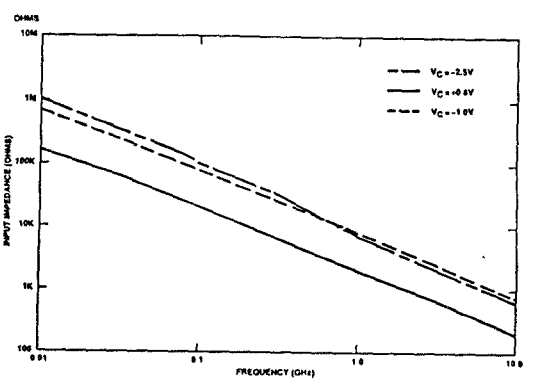

Figure 2.7 Computed current source (J9) impedance vs. frequency

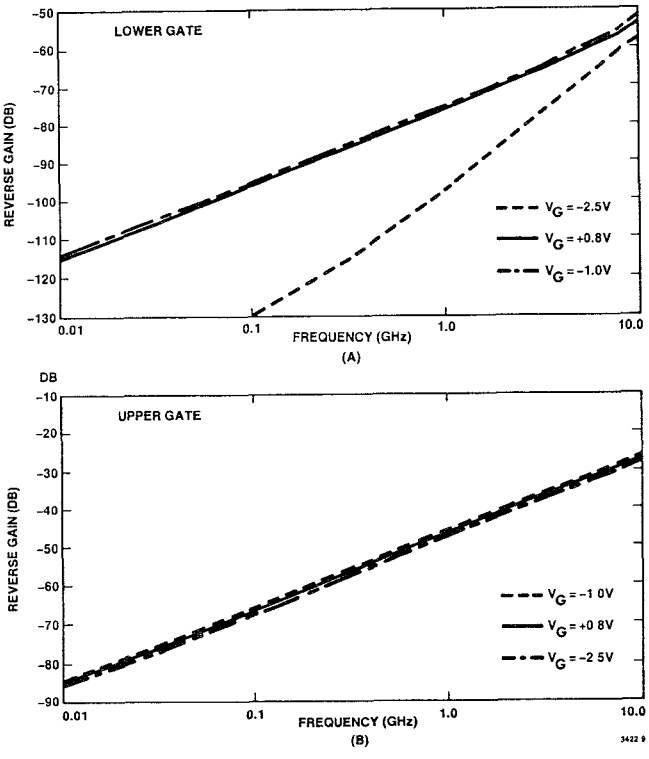

Figure 2.8 Computed input impedance of the RF port vs. frequency for various current sound gate voltages.

Chip Layout and Fabrication

Figure 3.1 shows a photograph of the multiplier chip, showing the layout configuration. As is customary, all MESFET's are layed out co-linearly to alliviate allignment constraints and to avoid transistor matching problems due to GaAs anisotropy. On this chip no second metal layer exists, so that several extra wire bonds are provided to accomplish the necessary inputs and outputs. In similar circuits which have been fabricated, second metal layer does exist.

The four guadrant multipliers were fabricated using standard processing technology (c.f. Figure 3.2). The n-type 800 ohm/sq, active layers were formed by vapor phase epitaxial growth of high resistivity GaAs substrates. A high resistivity buffer layer was interposed between the active layer and the substrate. The doping density of the active layer is 2×10^{17} cm^{-3}. The active areas of the FETs and resistors were defined using mesa etching. Source and drain ohmic contracts were formed by alloying evaporated AuGe/Ni at 460°C for 2.5 minutes. The gate and pad metallization was defined using evaporated Ti/Pt/Au and chlorobenzene assisted lift-off. The 1 micrometer gates are separated by 2 micrometers and centered in a 7.5 micrometer source-drain spacing. the 0.7 mm x 0.7 mm die is passivated with polyimide. Typical d.c. characteristics of the 75 micrometer wide, dual-gate MESFETs are V_p = 3.0 V, I_{DSS} = 15 ma, and g_m = 8 mS at 50% I_{DSS}.

Measured Results

The four quadrant multiplier chips were evaluated using the test fixture shown in Figure 4.1. Eight lead metal flat packs available from Mini Systems Inc. were mounted on Teflon circuit boards to provide a means of easily connecting and reconnecting chips for evaluation. Previous efforts had been made toward the fabrication of test fixtures employing ceramic substrates and die bonding the MMIC's directly to the ceramic. It was found that this process was very time consuming and not easily adaptable to testing of a large number of chips. The use of metal flatpacks in packaging of GaAs MMIC's has been reported on recently[5]. There it was indicated that using the 8 pin packages will allow for operation out to X band . We have found tht use of the type 5C8M (Mini Systems Inc.) flat packages provides adequate performance with the multiplier circuits out to about 8-10 GHz.

Circuit evaluation involved four areas of concentration. These were 1) D.C. transfer curves, 2) RF frequency response, 3) time domain (i.e., step response) measurements and 4) evaluation of the circuit as a modulator. The results of these measurements are discussed below:
1) D.C. Transfer Curves - The most important D.C. transfer curve relevant to the four quadrant multiplier is its square law performance. Measurements of the square law response by applying a ramp signal from a function generator to both inputs and observing the single ended output. The results of these measurements are shown on Figures 4.2a and 4.2b. Figure 4.2a shows the single ended output from the multiplier for differential input signal, taken at three different current source (MC) gate voltage values. Here, square law performance is clearly shown. Figure 4.2b, which shows single ended output

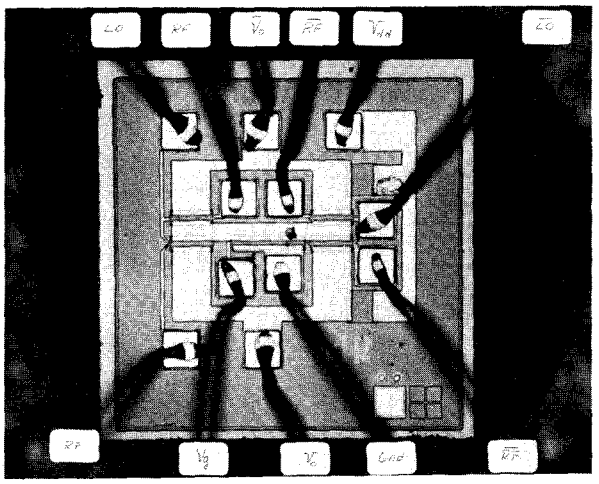

Figure 3.1 Photograph of the four quadrant multiplier

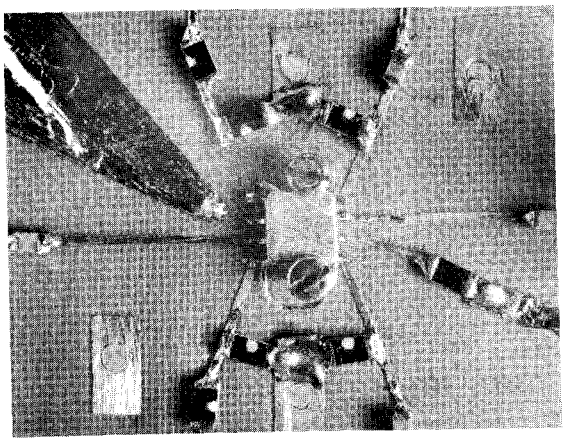

Figure 4.1 Photograph of test fixture used in RF measurements of the four quadrant multiplier

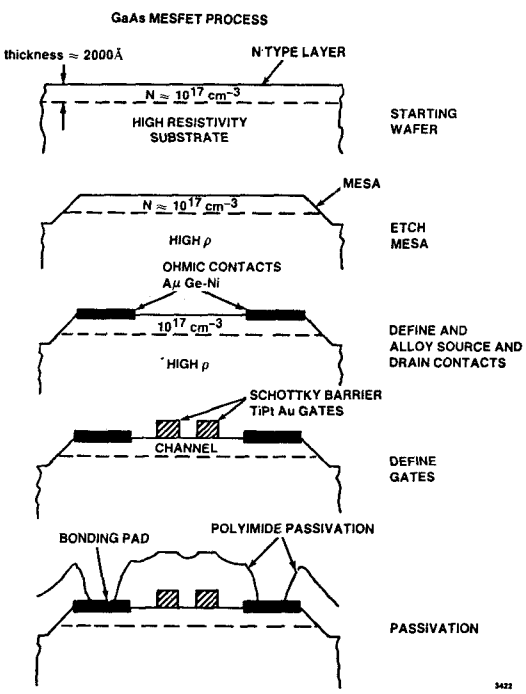

Figure 3.2 GaAs MESFET process flow

of the multiplier for single ended inputs shows deviations from square law performance, depending on the bias of the current source MC. This photograph indicates tht due to the insufficiently high impedance of MC, multiplier imbalance is introduced. As shown previously (Figure 2.7), addition of a source resistor at M9 will significantly enhance the impedance at the sources of the coupled pairs, thereby alleviating the imbalance problem significantly. We are currently designing new multiplier circuits which will embody this design improvement.

2) R.F. Frequency Response - RF response of the four quadrant multiplier is shown in Figure 4.3. here the LO port is used as a gate and the RF port is being driven by the RF signal. In one case the LO port is fully open and in the other case the LO port is fully pinched off. This then shows the on-off ratio of the multiplier as a function of frequency. As illustrated, flat response is obtianed out to 8 GHz and the on-off ratio is 20 dB at 2.5 GHz and 12 dB at 8 GHz. Measurements were made by driving the multiplier into a 50Ω load. As shown in Figure 4.3 the MESFET's were not of sufficient width in this lot of chips to provide gain, however, follow-on designs to be obtained soon will be of sufficient size to provide some useful gain into 50Ω.

3) Time Domain Response - step resonse of the multiplier is shown in Figure 4.4. Here the step pulse was applied to the RF port and the LO port was applied to several D.C. voltages. As shown, the multipliers rise time is approximately 50 ps.
4) Modulator Evaluation - To evaluate the performance of the circuit as a balanced modulator a 10 MHz square pulse was applied at the LO port and a 250 MHz sine wave was applied at the RF port. The output frequency spectrum was then measured. This measurement is shown in Figure 4.5. Noteworthy in this photograph is the 10 dB suppression of the carrier, giving a measure of the balance of the modulator. As mentioned eailer, later version of this circuit will include a source resistance of approximately 100 in the current source transistor MC. It is expected that this will help to improve the carrier suppression capability of the circuit.

Conclusion

The GaAs MMIC four quadrant multiplier has been demonstrated as a viable alternative to the more convetional discrete circuit diode mixer. This circuit offers the advantage of small sizes, conversion gain, and unilateral signal flow.

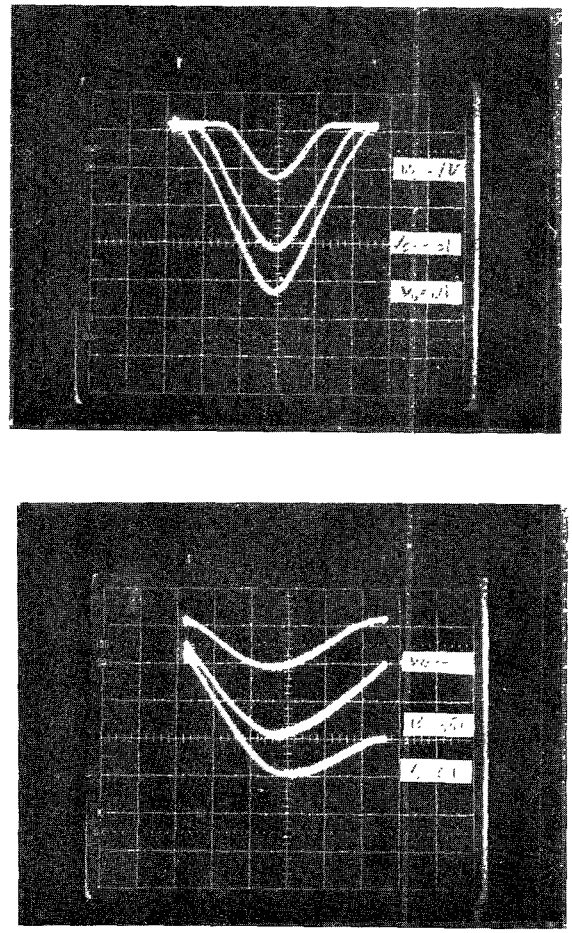

Figure 4.2 Measured differential (a) and single ended (b) square law response of the four quadrant multiplier

References

(1) K.P. Weller, N. Duttathriya, T.S Lin, Technical Digest, GaAs IC Symposium, New Orleans, LA., Nov. 9, 10,11, pg.75.

(2) Ryan, C., U.S. Patent #3,452,289

(3) Musatti, B., "Analysis ofa GaAs FET Four Quadrant Multiplier", MSEE Thesis Arizona State University, Dec. 1980.

(4) W.R. Curtice, IEEE Trans. Microwave Th. & Tech., 28, 5,& 48, May 1980.

(5) D.W. Wilson, N. Frick, J. Kwiat, S. Lo, J. Churchill, J. Berrera; Technical Digest, GaAs IC Symposium, New Orleans, LA., Nov. 9, 10, 11, pg.13.

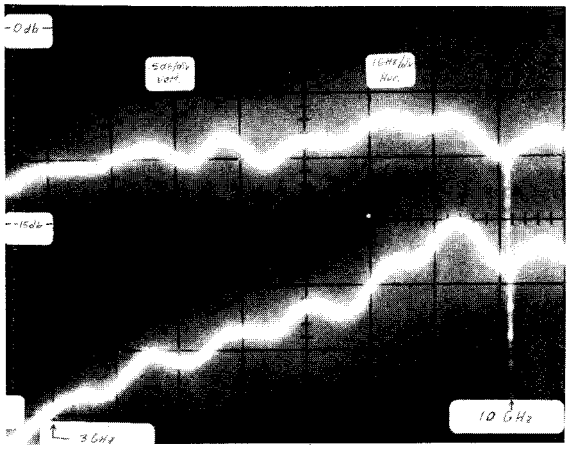

Figure 4.3 RF frequency response of the multiplier, showing its on/off ratio vs. frequency

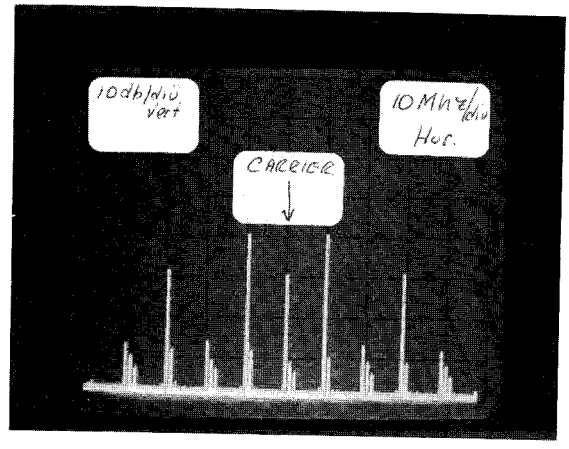

Figure 4.5 Response of the multiplier circuit when used as a balanced modulator

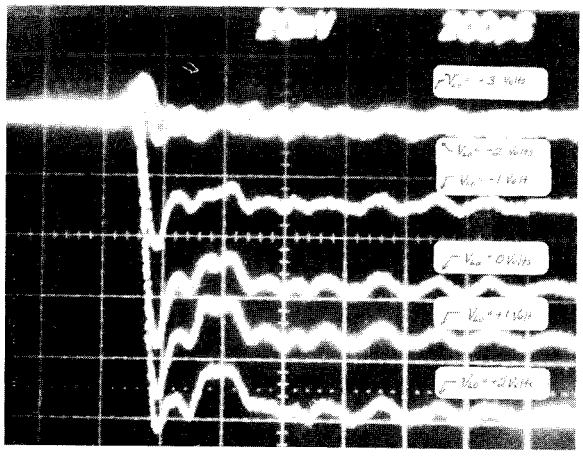

Figure 4.4 Step response of the multiplier circuit